REMARKS

Reconsideration of the application in view of the above amendments and following remarks is respectfully requested. Claim 6 has been amended to clarify its scope, and Claims 15-17 have been added. Claims 1-17 are pending in the application.

Claim Rejections under 35 U.S.C. §102(e)

In the above Office Action dated October 7, 2003, the Examiner rejected pending claims 1-14 under 35 U.S.C. §102(e) as being unpatentable over Yamashita et al. (US 6,564,343). Applicant respectively traverses this rejection.

The Examiner contends that Yamashita et al.'s RAMs 42#0, 42#1, 110#0, 110#1 shown in FIG. 3 correspond to Applicant's memory buffer, and presumably contends that Yamashita et al.'s first and second deinterleave means 66, 68 correspond to Applicant's recited means for performing a first and second de-interleaving of the data (See Office Action mailed October 7, 2003 pages 3 and 4).

Applicant respectfully disagrees and submits that Applicant's claimed first and second de-interleaving is very different in many respects from the deinterleaving described by Yamashita et al. For example, Yamashita et al. teach the deinterleaving of two different signals: a received signal and a command signal. The command signals are generated based upon the reception level of each bit of the received signal (See FIG. 1 and Col. 5, lines 35-43). Specifically, Yamashita et al. teach that the "first deinterleave means 66 deinterleaves the received signal completing a bit interleave process by rearranging bits in the signal, and the second deinterleave means 68 rearranges command signals to output the command signals according to bits of a signal output by the first deinterleave means 66." (See Col. 6, lines 1-5).

In contrast, Applicant's independent claims 1, 6 (as amended), and 9 each recite performing both "a first and second deinterleaving of the data." Although Yamashita et al. teach two deinterleaver means 66, 68, Yamashita et al. neither teaches nor suggests that their received signal or their command signal undergo both "a first and second deinterleaving" as recited in independent claims 1, 6 (as amended) and 9. As a consequence Yamashita et al. does not anticipate independent claims 1, 6 and 9.

With respect to independent claims 11 and 13, the Examiner has not shown where each and every step of these method claims is taught by Yamashita et al. Instead, the Examiner rejects claims 11 and 13 on the basis that the Abstract of Yamashita et al. shows first and second deinterleave units and Col. 5. lines 43-47 together with Col. 6, lines 55-67 show a memory buffer for performing a first and second deinterleaving of data in the memory buffer (See Office Action dated October 7, 2003. para. 7, page 4). Assuming arguendo, that the Examiner is correct, the examiner has not made a prima facie case that Yamashita et al. anticipates claim 11 because the Examiner does not even allege that Yamashita et al. teaches or suggests "performing a second de-interleaving as the data is written to a memory buffer; and performing a first de-interleaving as data is read from said memory buffer" as recited in claim 11.

Moreover, the Examiner has not made a prima facie case that Yamashita et al. anticipates claim 13 because the Examiner does not even allege that Yamashita et al. teaches or suggests "writing said data to a memory buffer according to a second deinterleaving pattern; and reading said data from said memory buffer according to a first de-interleaving pattern" as recited in claim 13. Thus, Applicant respectfully requests that the Examiner identify each and every element recited in Claims 11 and 13 in Yamashita et al. or remove the rejection.

Moreover Applicant submits that Yamashita et al. does not suggest carrying out a first and second deinterleaving of data because that would destroy the operability of their receiver. Namely, Yamashita et al.'s transmitters (described with reference to FIGS. 2, 8 and 10, 12, 14, 15, 16, 19, 20, 21, 22 and 24) do not carry out a first and second interleaving of their data; thus, if a first and second deinterleaving were performed on their interleaved data, it would result in unintelligible data.

Thus, Applicant submits independent claims 1, 6, 9, 11 and 13 are novel and non-obvious, and respectfully requests that the Examiner reconsider the outstanding rejection with a view towards allowance of claims 1, 6, 9, 11 and 13.

In view of the remarks above, Applicant further submits that dependent claims 2-5, 7-8, 10, 12 and 14 are allowable by virtue of their dependence on one of the allowable independent claims 1, 6, 9, 11 and 13.

Applicant also submits that new claims 15-17 are allowable because they claim that which is not shown nor suggested by the prior art for the reasons set forth above. Claims 15-17 are supported by the Specification as filed and, at least, claims 1-3 and 6.

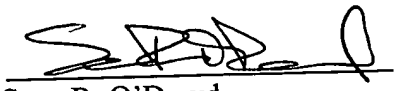
CONCLUSION

Applicant respectfully requests entry of these amendments prior to the examination of the above-identified application. Applicant respectfully submits that the invention as presently claimed is patentably distinct from the cited references, either alone or in combination. The undersigned would of course be available to discuss the present application with the Examiner if in the opinion of the Examiner such a discussion could advance prosecution of the present application.

Dated: January 6, 2004

Respectfully submitted,

COOLEY GODWARD LLP



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